



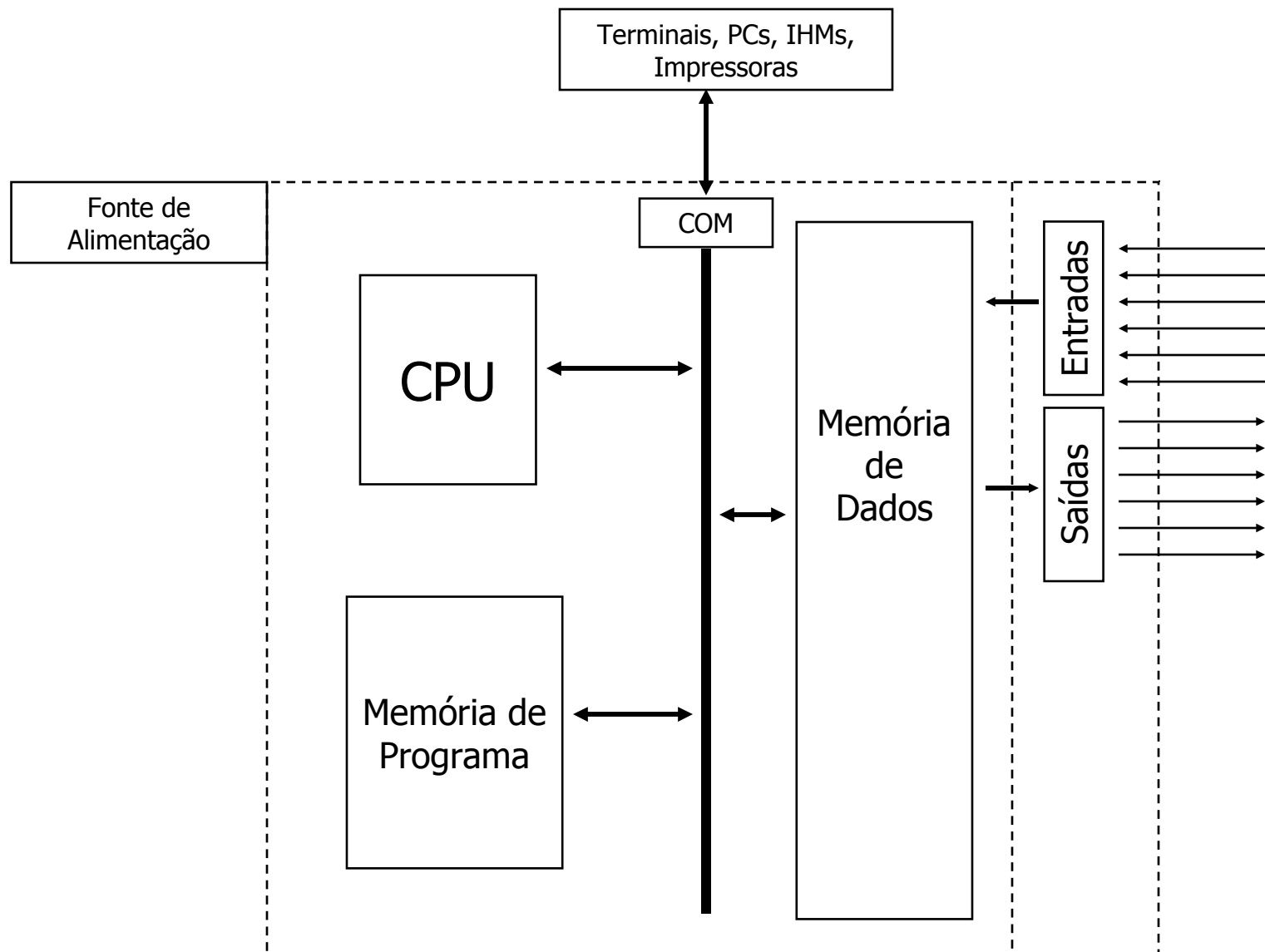
# Lógica de Controle

# CLPs

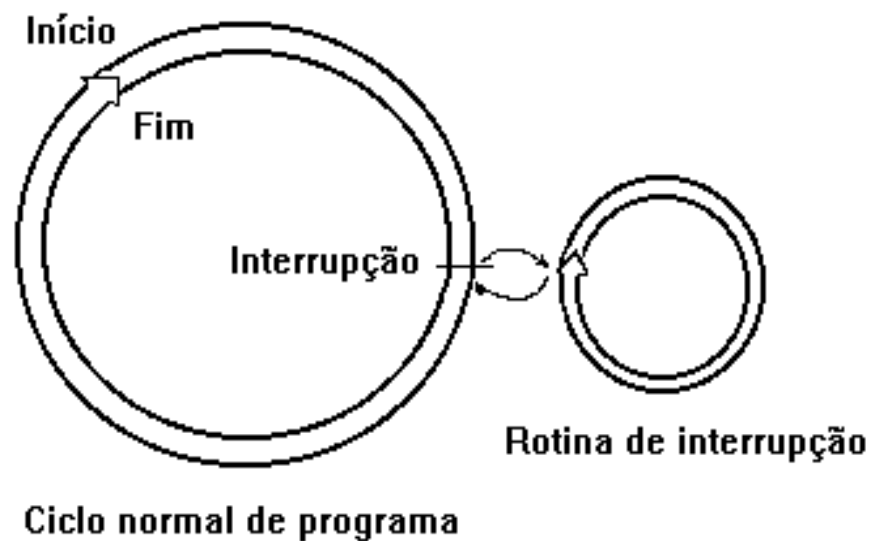
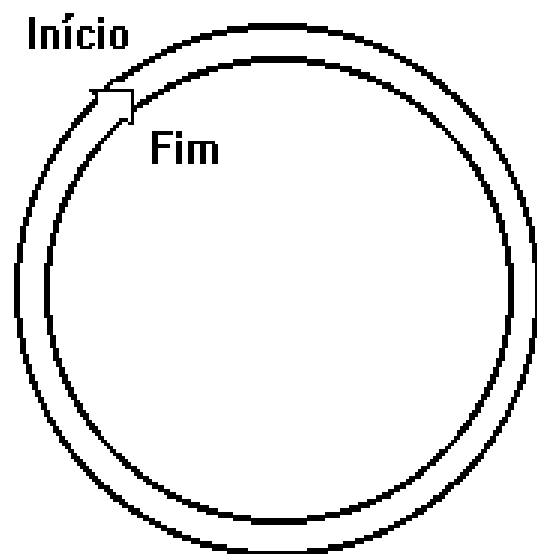
## Vantagens do uso de Controladores Lógicos Programáveis

- Ocupam menor espaço;
- Requerem menor potência elétrica;
- Podem ser reutilizados;
- São programáveis, permitindo alterar os parâmetros de controle;
- Apresentam maior confiabilidade;
- Manutenção mais fácil e rápida;
- Oferecem maior flexibilidade;
- Apresentam interface de comunicação com outros CLP's e computadores de controle;
- Permitem maior rapidez na elaboração do projeto do sistema.

# Arquitetura do CLP



# CPU

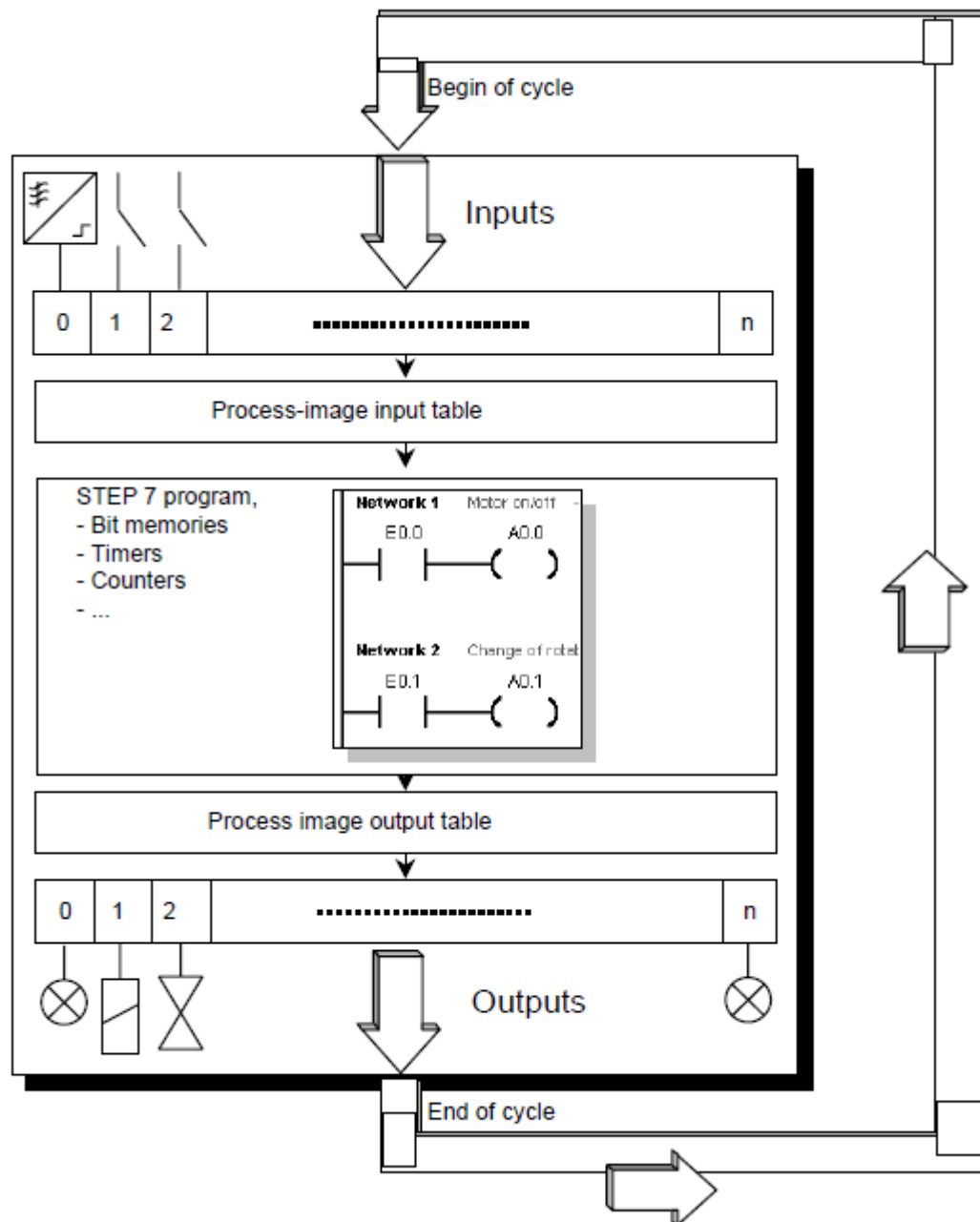


INSTITUTO FEDERAL  
SANTA CATARINA  
Campus Araranguá

# CPU



# CPU

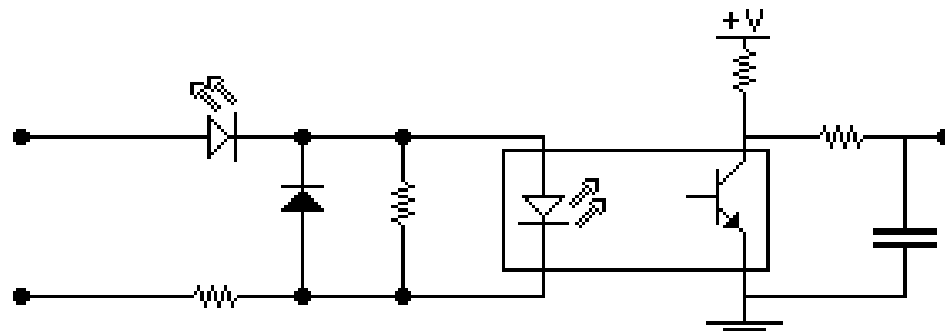


# Memória

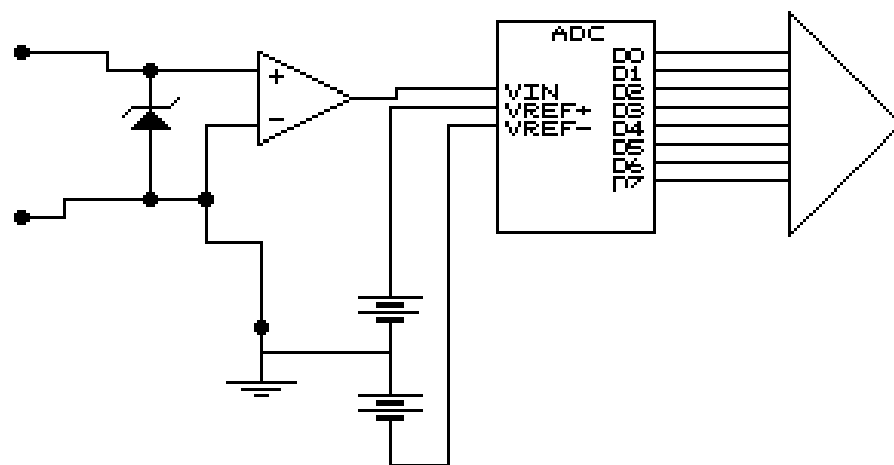
<i>Tipo de Memória</i>	<i>Descrição</i>	<i>Observação</i>
<b>RAM DINÂMICA</b>	Memória de acesso aleatório	<ul style="list-style-type: none"><li>- Volátil</li><li>- Gravada pelo usuário</li><li>- Lenta</li><li>- Ocupa pouco espaço</li><li>- Menor custo</li></ul>
<b>RAM</b>	Memória de acesso aleatório	<ul style="list-style-type: none"><li>- Volátil</li><li>- Gravada pelo usuário</li><li>- Rápida</li><li>- Ocupa mais espaço</li><li>- Maior custo</li></ul>
<b>ROM MÁSCARA</b>	Memória somente de leitura	<ul style="list-style-type: none"><li>- Não Volátil</li><li>- Não permite apagamento</li><li>- Gravada pelo fabricante</li></ul>
<b>PROM</b>	Memória programável somente de leitura	<ul style="list-style-type: none"><li>- Não volátil</li><li>- Não permite apagamento</li><li>- Gravada pelo usuário</li></ul>
<b>EPROM</b>	Memória programável/apagável somente de leitura	<ul style="list-style-type: none"><li>- Não Volátil</li><li>- Apagamento por ultravioleta</li><li>- Gravada pelo usuário</li></ul>
<b>EPROM EEPROM FLASH EPROM</b>	Memória programável/apagável somente de leitura	<ul style="list-style-type: none"><li>- Não Volátil</li><li>- Apagável eletricamente</li><li>- Gravada pelo usuário</li></ul>

# Entradas

Entrada Digital

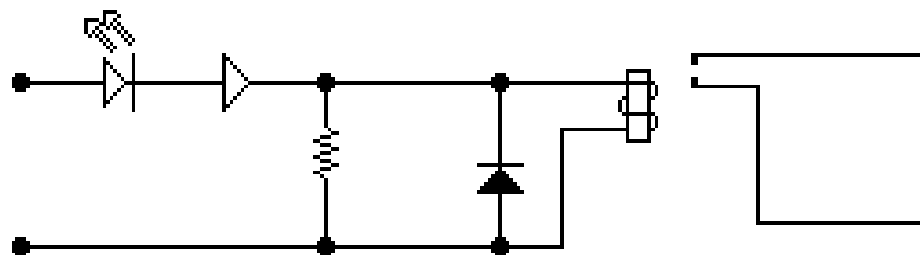


Entrada Analógica

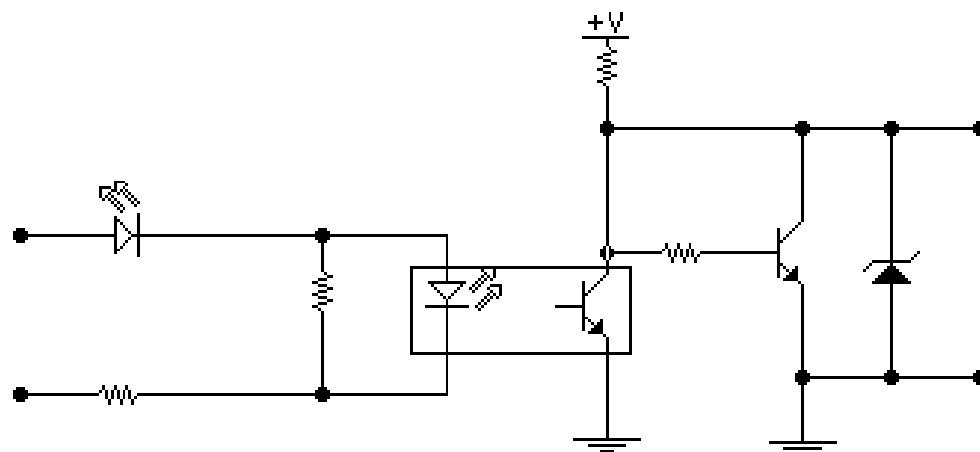




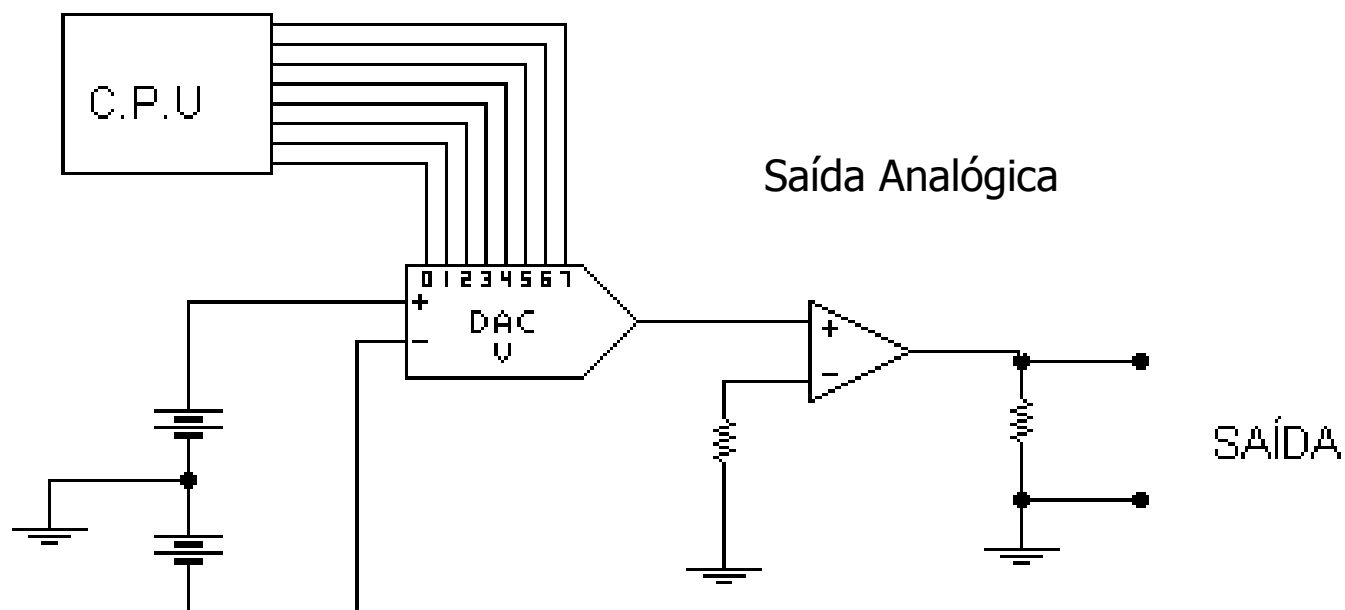
Saída Digital  
à Relê



Saída Digital  
à Transistor



# Saídas



# Tecnologias Industriais

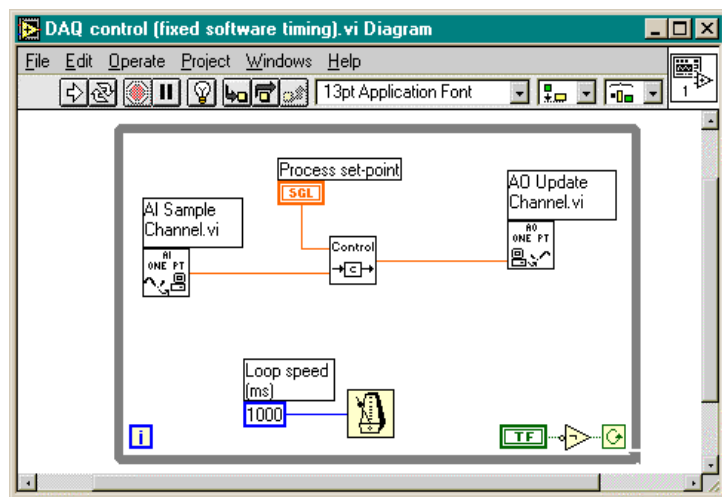


## Sistema Field Point

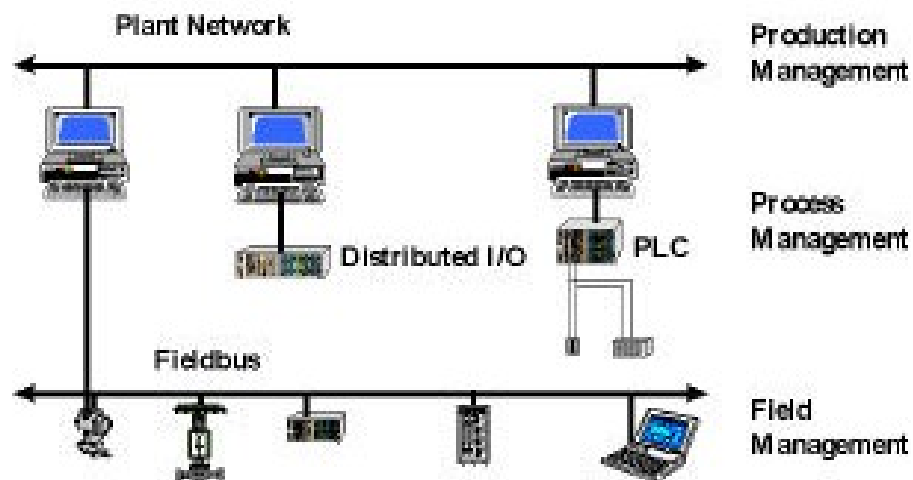


INSTITUTO FEDERAL  
SANTA CATARINA  
Campus Araranguá

# Tecnologias Industriais

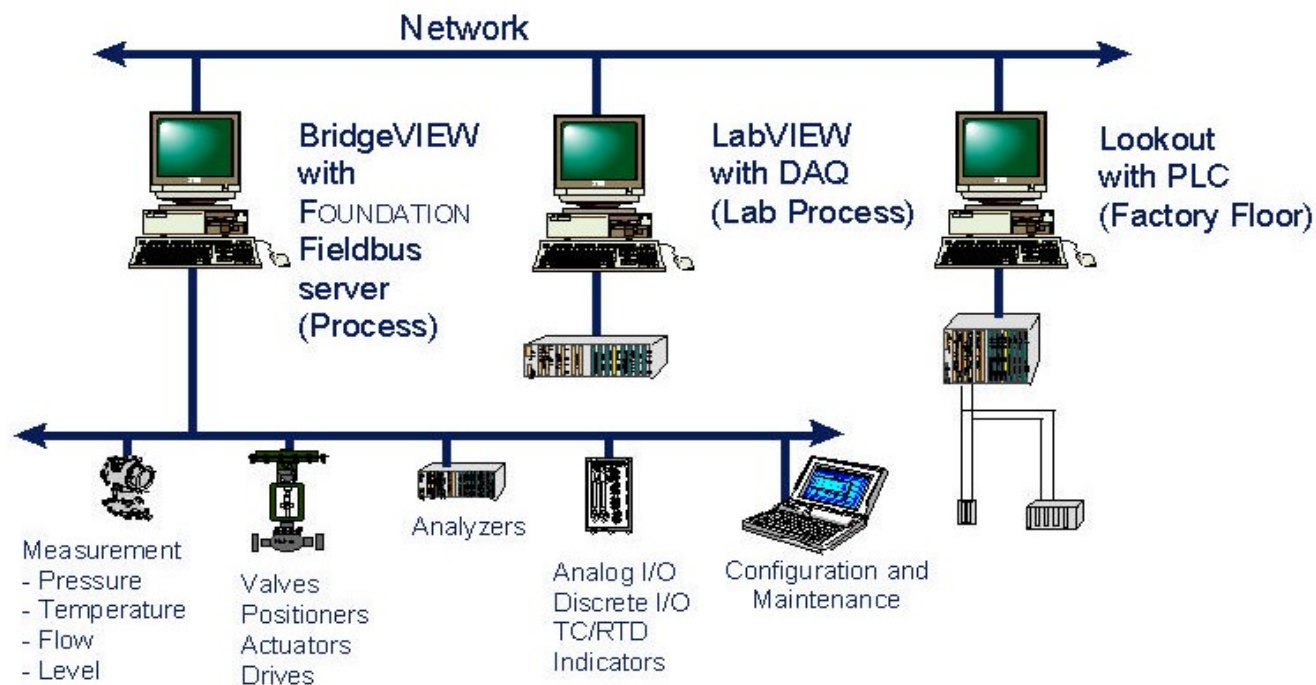


## Arquitetura BridgeVIEW

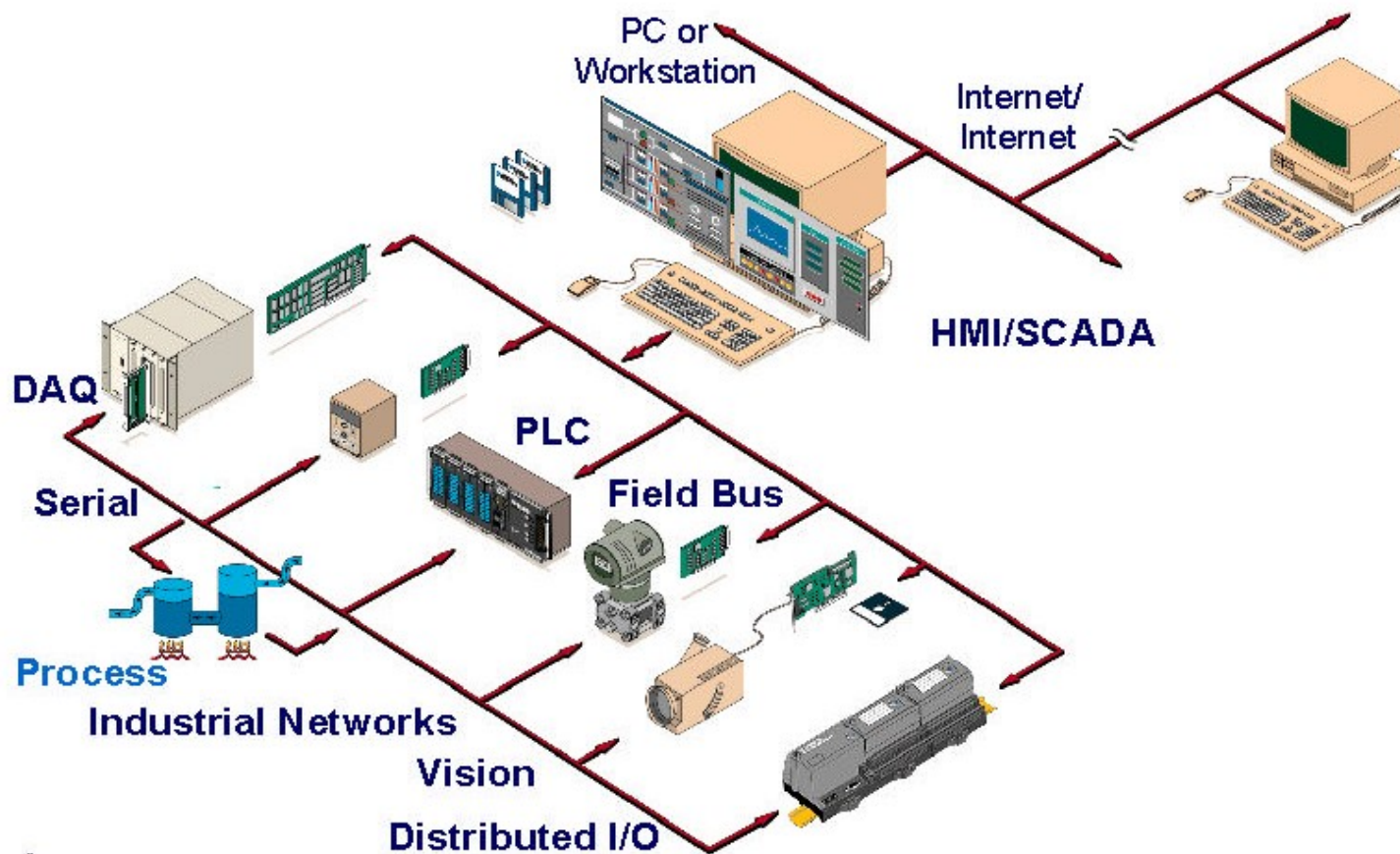


# Tecnologias Industriais

## Aplicações de Automação



# Tecnologias Industriais



# CLPs Comerciais

Pequeno Porte (Micro CLP)  
Até 320 E/S



CLP de Médio Porte  
Até 2500 E/S



CLP de Grande Porte  
Até 5000 E/S



INSTITUTO FEDERAL  
SANTA CATARINA  
Campus Araranguá



# CLPs Comerciais



BOSCH

New!



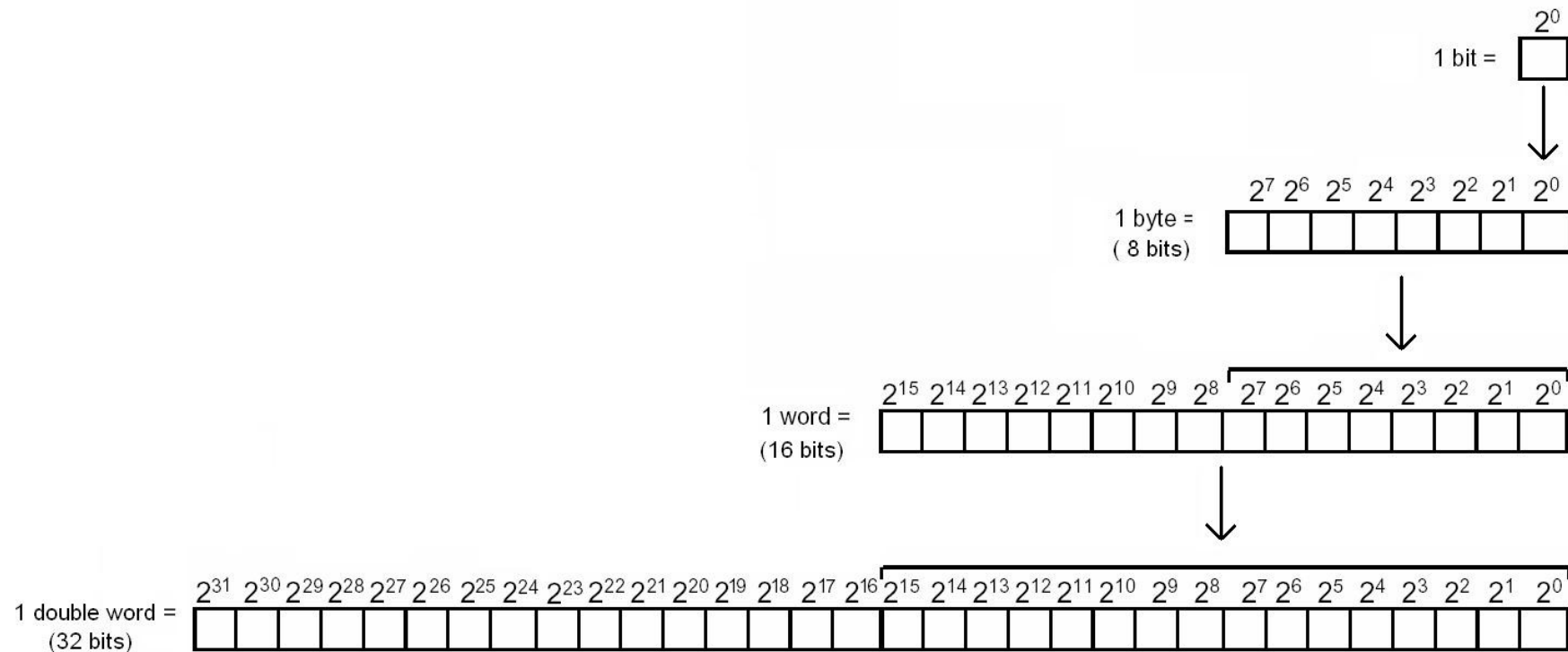
Micro  
CLP  
Linha  
TP 02



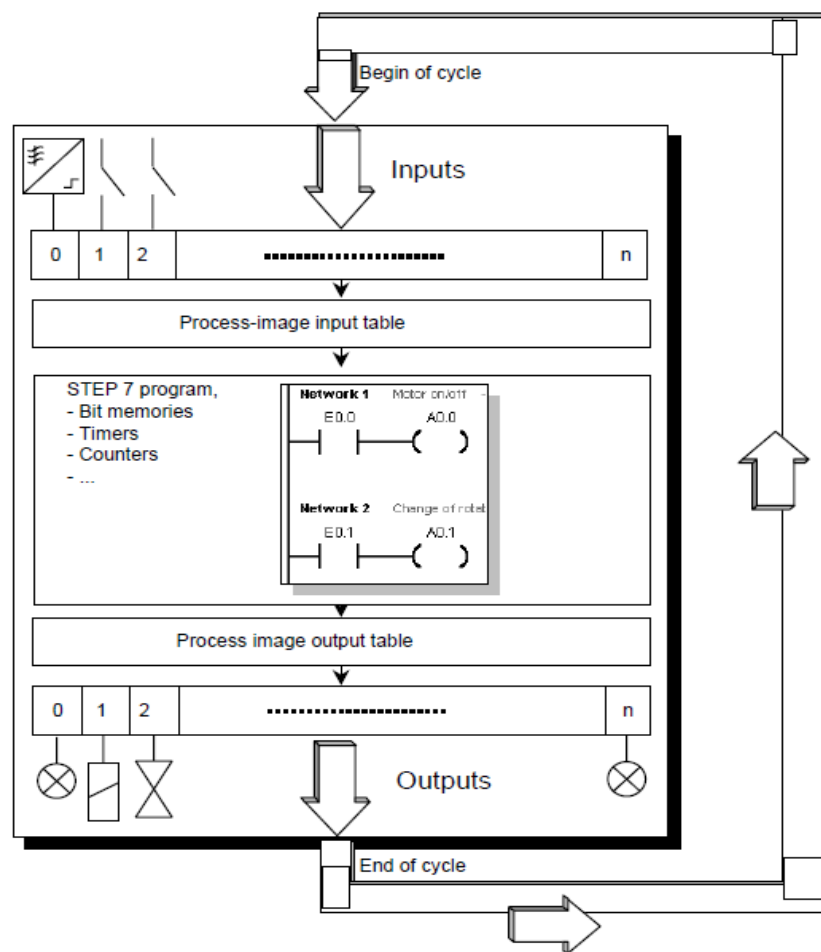
INSTITUTO FEDERAL  
SANTA CATARINA  
Campus Araranguá



# Estrutura de Dados



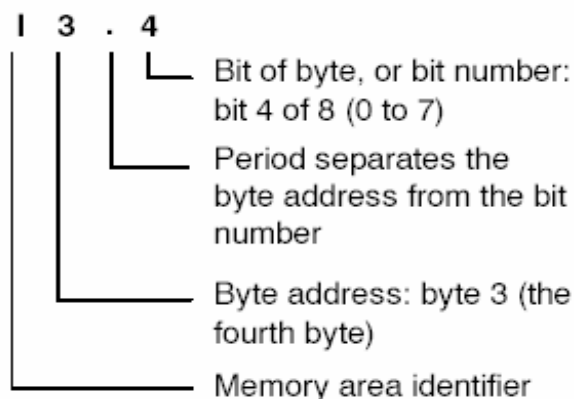
# Estrutura de Dados



# Estrutura de Dados

Representation	Byte (B)	Word (W)	Double Word (D)
Unsigned Integer	0 to 255 0 to FF	0 to 65,535 0 to FFFF	0 to 4,294,967,295 0 to FFFF FFFF
Signed Integer	-128 to +127 80 to 7F	-32,768 to +32,767 8000 to 7FFF	-2,147,483,648 to +2,147,483,647 8000 0000 to 7FFF FFFF
Real IEEE 32-bit Floating Point	<i>Not applicable</i>	<i>Not applicable</i>	+1.175495E-38 to +3.402823E+38 (positive) -1.175495E-38 to -3.402823E+38 (negative)

To access a bit in a memory area, you specify the address, which includes the memory area identifier, the byte address, and the bit number. Figure 4-3 shows an example of accessing a bit (which is also called “byte.bit” addressing). In this example, the memory area and byte address (I = input, and 3 = byte 3) are followed by a period (“.”) to separate the bit address (bit 4).



Process-image Input (I) Memory Area

	7	6	5	4	3	2	1	0
Byte 0								
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5								



# Estrutura de Dados

- **TIPOS DE ENDEREÇOS**

- **I** = DIGITAL INPUT
- **Q** = DIGITAL OUTPUT (QUIT)
- **AIW** = ANALOG INPUT
- **AQW** = ANALOG OUTPUT (QUIT)
- **V** = VARIABLE (FLAG)
- **M** = MEMORY
- **C** = COUNTER
- **T** = TIMER

# Estrutura de Dados

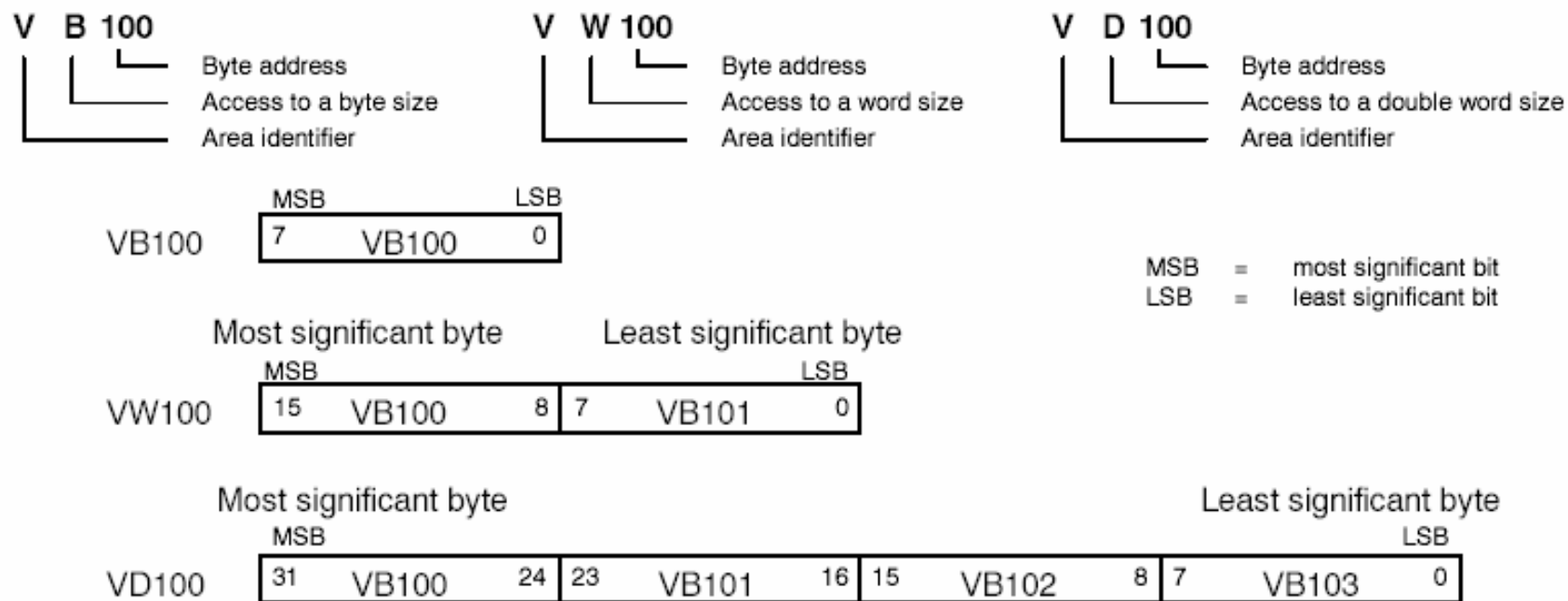
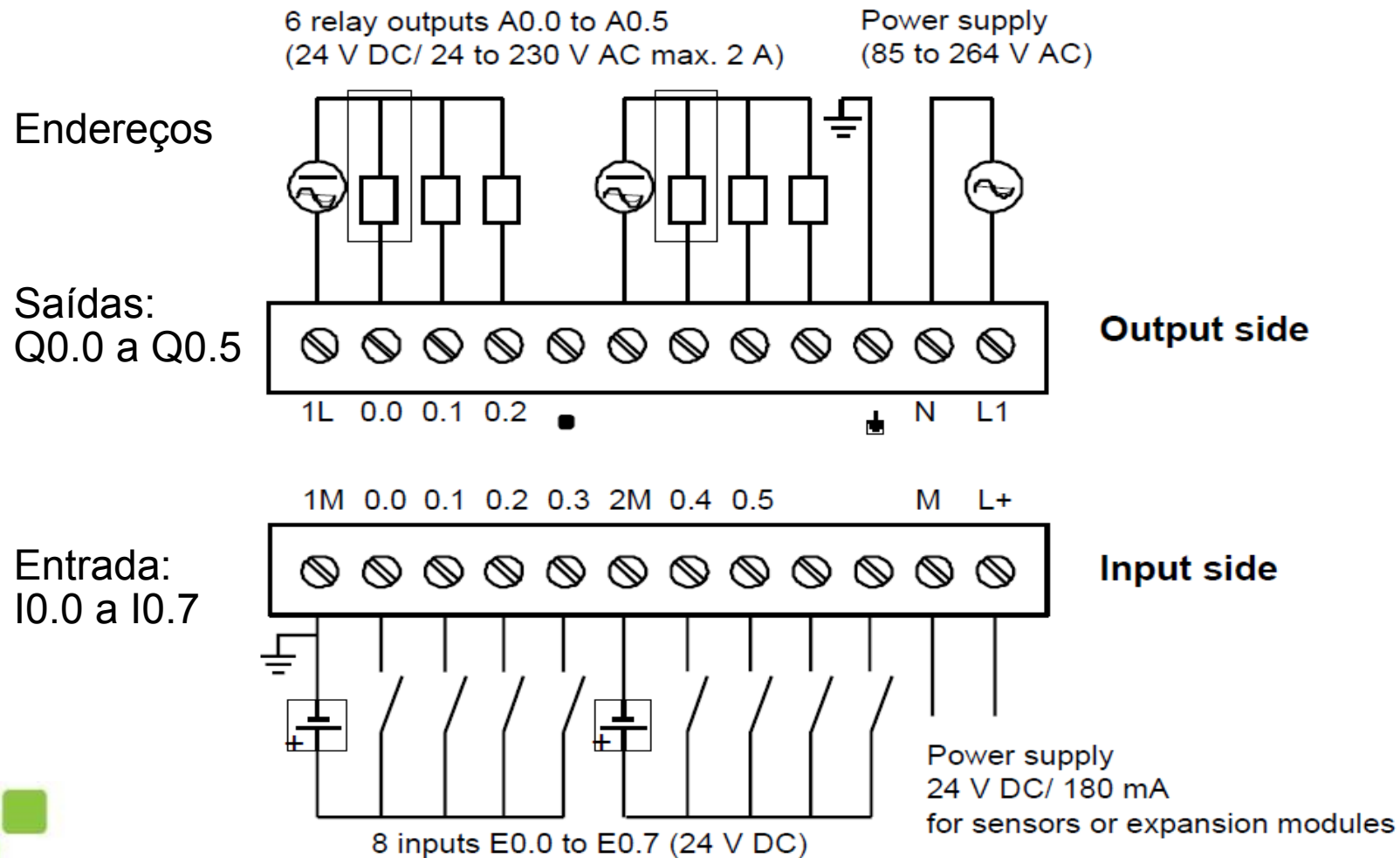
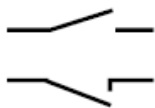

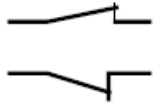

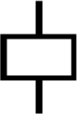
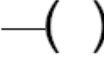
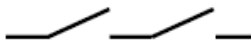
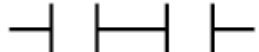
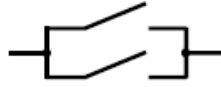
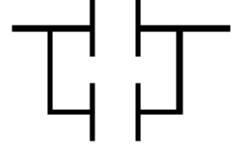


Figure 4-4 Comparing Byte, Word, and Double-Word Access to the Same Address

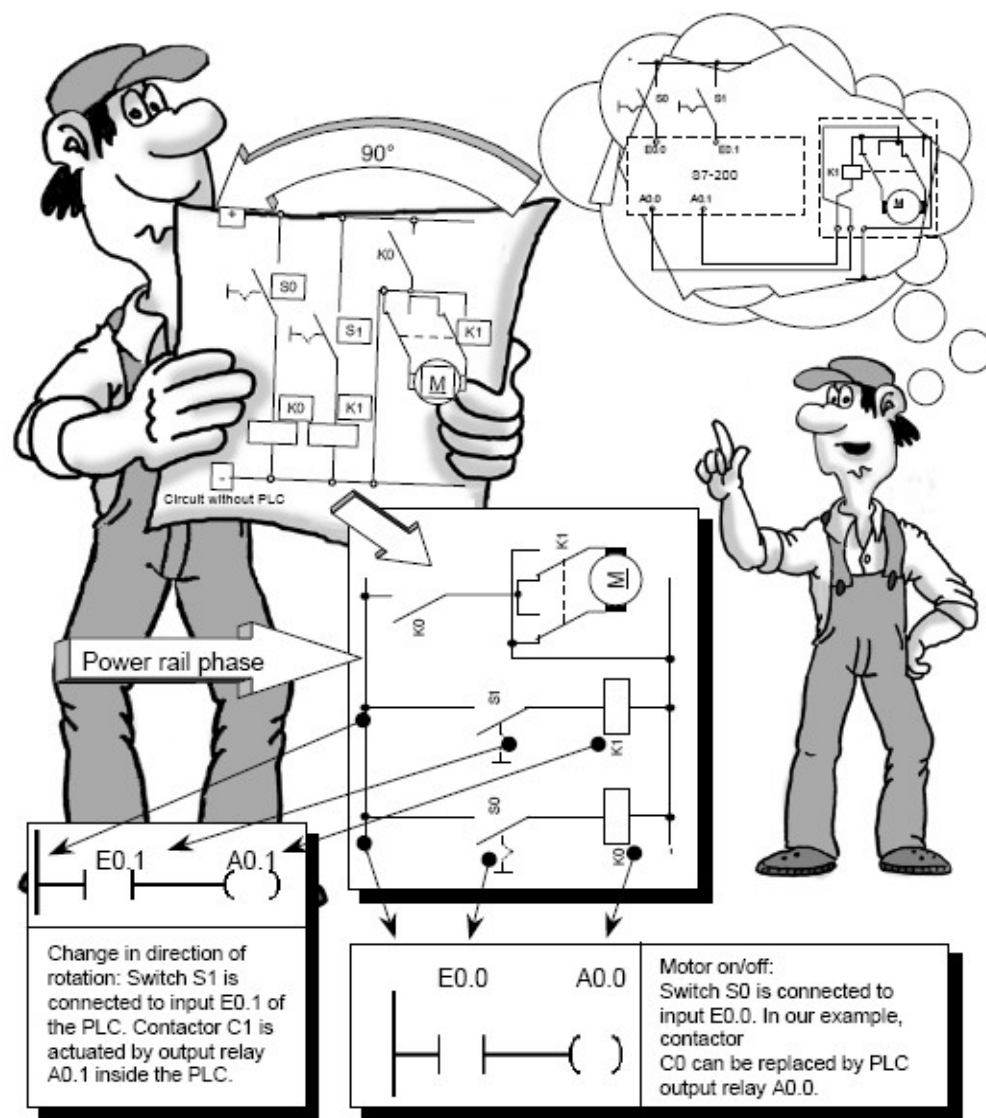
# Estrutura de Dados



# Linguagem Ladder

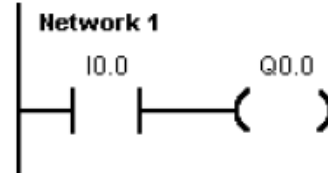
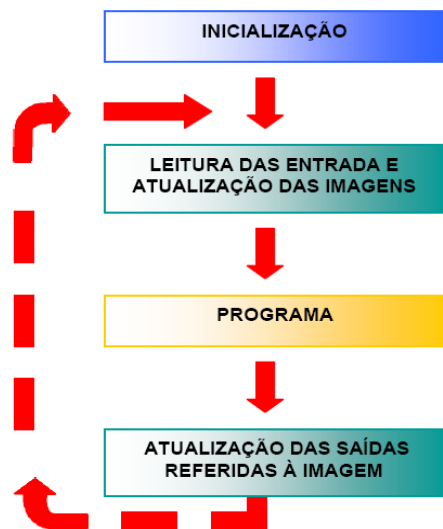
Contactor	Instruction on the PLC/ corresponding function	
	Scan: Is current flowing ? If yes, then the result of the scan is true. (Result is "1")	
	Scan: Is <u>no</u> current flowing ? If yes (no current), then the result of the scan is true. (Result is "0")	
	Coil: If the value "true" (current) is passed to a coil it is activated (The coil starts up).	
	Series circuit: (AND logic). The first switch AND the second switch must be closed in order to pass current.	
	Parallel circuit (OR logic). The first switch OR the second switch must be closed in order to pass current.	

# Linguagem Ladder





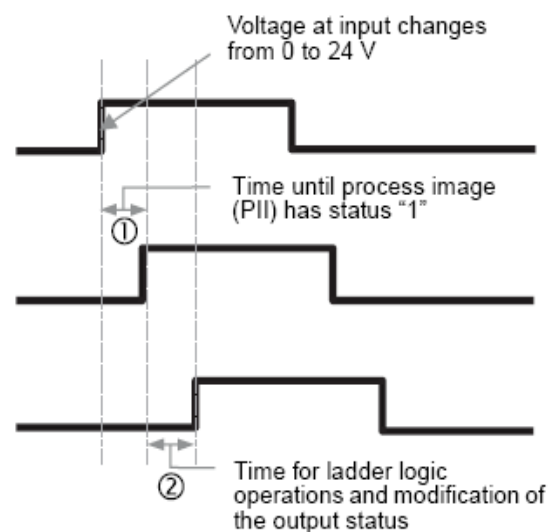
# Linguagem Ladder



State of input  
I0.0

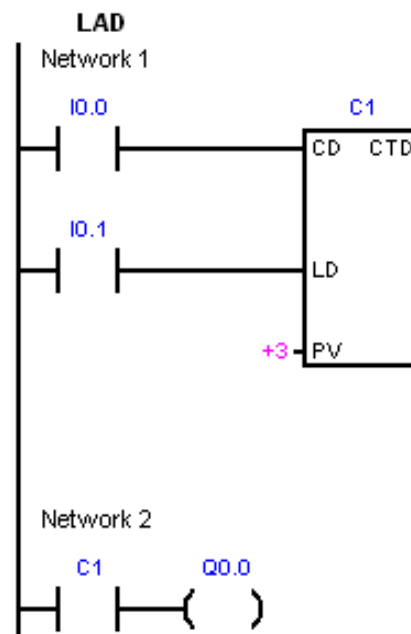
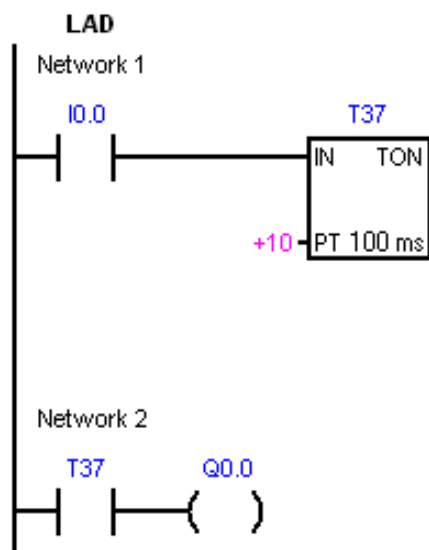
Process-  
image of I0.0

State of output  
Q0.0



INSTITUTO FEDERAL  
SANTA CATARINA  
Campus Araranguá

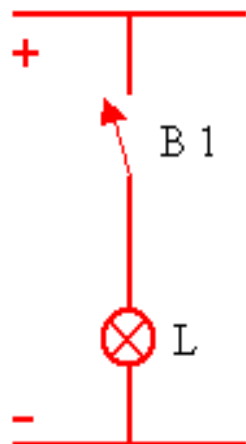
# Linguagem Ladder



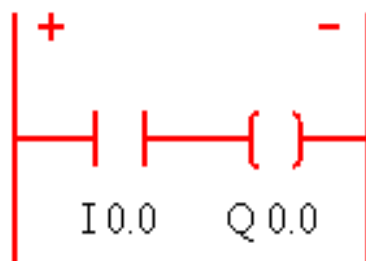
# Linguagem Ladder

- *definição da função lógica a ser programada*
- *transformação desta função em programa assimilável pelo CLP*
- *implementação física do controlador e de suas interfaces com o processo*

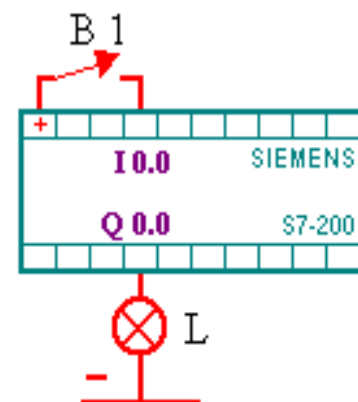
Circuito elétrico



Programa

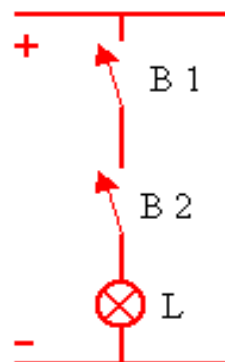


Circuito CLP

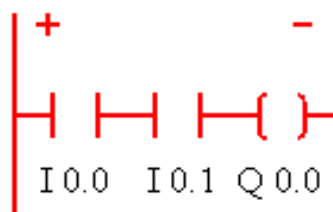


# Linguagem Ladder

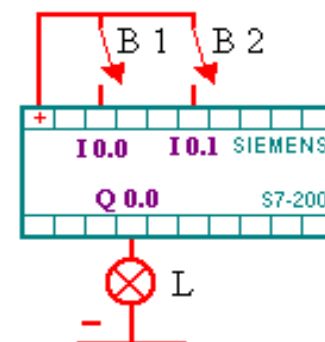
Circuito elétrico



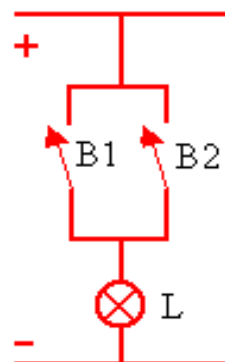
Programa



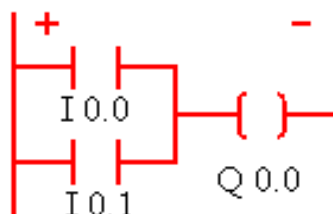
Circuito CLP



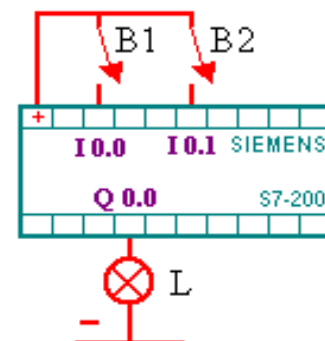
Circuito elétrico



Programa

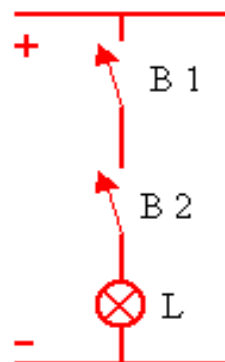


Circuito CLP

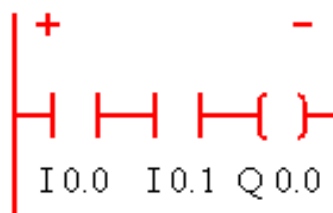


# Linguagem Ladder

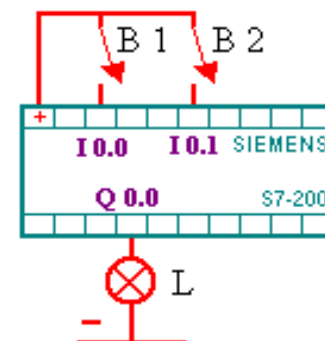
Circuito elétrico



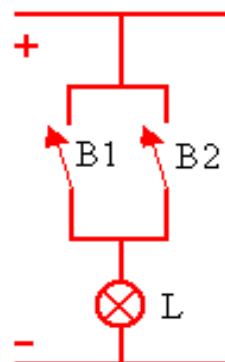
Programa



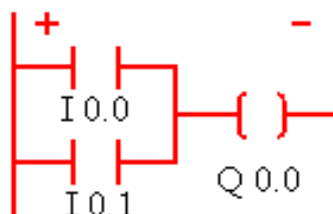
Circuito CLP



Circuito elétrico



Programa



Circuito CLP

